PRO-LOG CORPORATION

STD 7000

7704 BYTE-WIDE Memory Card

USER'S MANUAL

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7704
BYTE-WIDE
Memory Card

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PRELIMINARY

1/82

FOREWARD

This manual explains how to use Pro-Log's 7704 Byte-Wide Memory Card It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7704. We welcome your suggestions on how we can improve our instructions.

The 7704 is part of pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of utilizing his own people to control the design, production, and maintenance of the company's proucts that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use, microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: *Microprocessor User's Guide* and the *Series 7000 STD BUS Technical Manual.* If you would like a copy of these documents, please submit your request on your company letterhead.

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The 7704 Byte-Wide Memory card is designed to be a flexible part of the memory in your system. Its eight sockets, designed for devices conforming to the JEDEC 28 pin dual inline standard pinout, allow the use of 2K, 4K, and 8K ROMs and RAMS all of one size or in combinations.

The card can respond the the STD BUS MEMEX line in one of two ways. The memory on the card can be separated into two banks, each bank selected by the MEMEX line. This allows up to 64K on one card. Alternately, two cards, with up to 64K on each card, can be used in a system, each card selected by the MEMEX line.

The MEMEX line can be used to implement a maximum of memory with a minimum of cards. A system using Pro-Log's 7804 Z80A processor card, and two 7704 cards, can have up to 124K of memory with no additional signal lines or cards.

The 7704 can also respond to an external Segment Select line, allowing it to participate in large scale bank select schemes. The Segment Select line can be controlled by a memory segment controller or by I/O ports. One output port can control eight 7704 cards. Also, it can be tailored to fit small scale applications. Unused sockets can be disabled, allowing the card to occupy as little as 2K bytes of memory space which can be mapped anywhere within a 64K byte address field.

The 7704 has 12 specific jumper-selectable combinations for memory parts. Some of these are designed to complement the memory provided on Pro-Log processor cards. Any of the memory parts can be either ROM or RAM. The address decoder for the specific memory configurations is a PROM, which can be reprogrammed by the user to provide any combination desired.

Features

* **All one size or combinations 2K, 4K, and 8K ROMs and RAMs**
* **28 pin JEDEC standard sockets**
* **Responds to STD BUS MEMEX line**
* **Responds to external Segment Select line**
* **Onboard flexible address decoding**
* **Processor independent -use with 8085, Z80, 6800, 6809, 8088 and others**

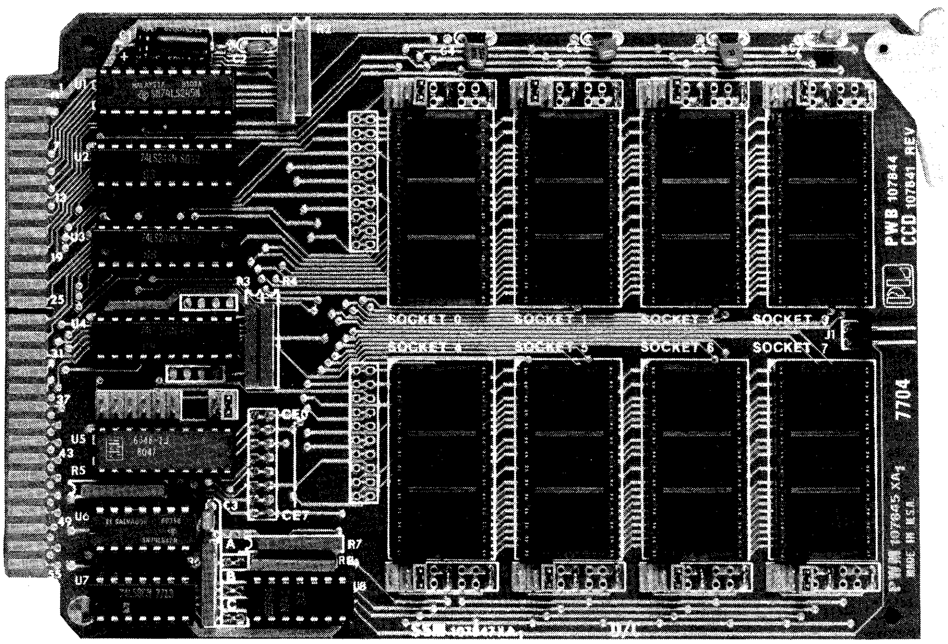


Figure 1-1. 7704 BYTE-WIDE Memory Card

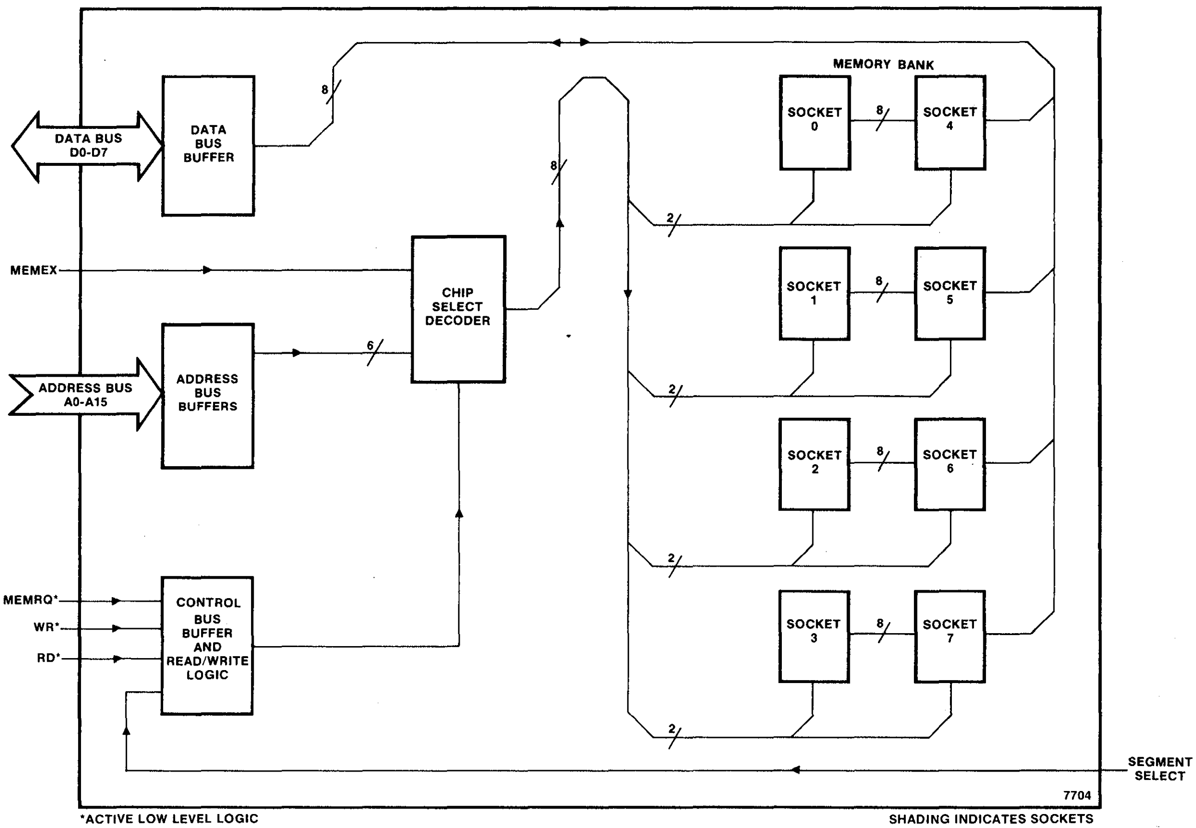


Figure 1-2. Block Diagram of 7704 BYTE-WIDE Memory Card

Installation and Specification

Installation

The 7704 operates as part of an STD BUS card rack system. You can plug it directly into the STD BUS backplane, as shown in Fig. 2-1, or extend it from the motherboard with a 7901 card extender. To use the 7901 card extender, plug it into any slot in the card rack, and plug the 7704 into the connector on the 7901 card. This makes the 7704 accessible for testing, etc.

The 7704 can occupy any slot in the card cage. It should be installed with the card ejector towards the top of the card rack as shown in Fig. 2-1.

If the external Segment Select line is used, it should be attached as shown in Fig. 2-2. The connector type is a 2-pin 0.1 inch center connector. The cable should be a twisted pair, consisting of one signal line and one ground line for added noise immunity. The Pro-Log RC704 cable can be used for this purpose and can connect the 7704 card to an I/O card such as Pro-Log's 7605 card.

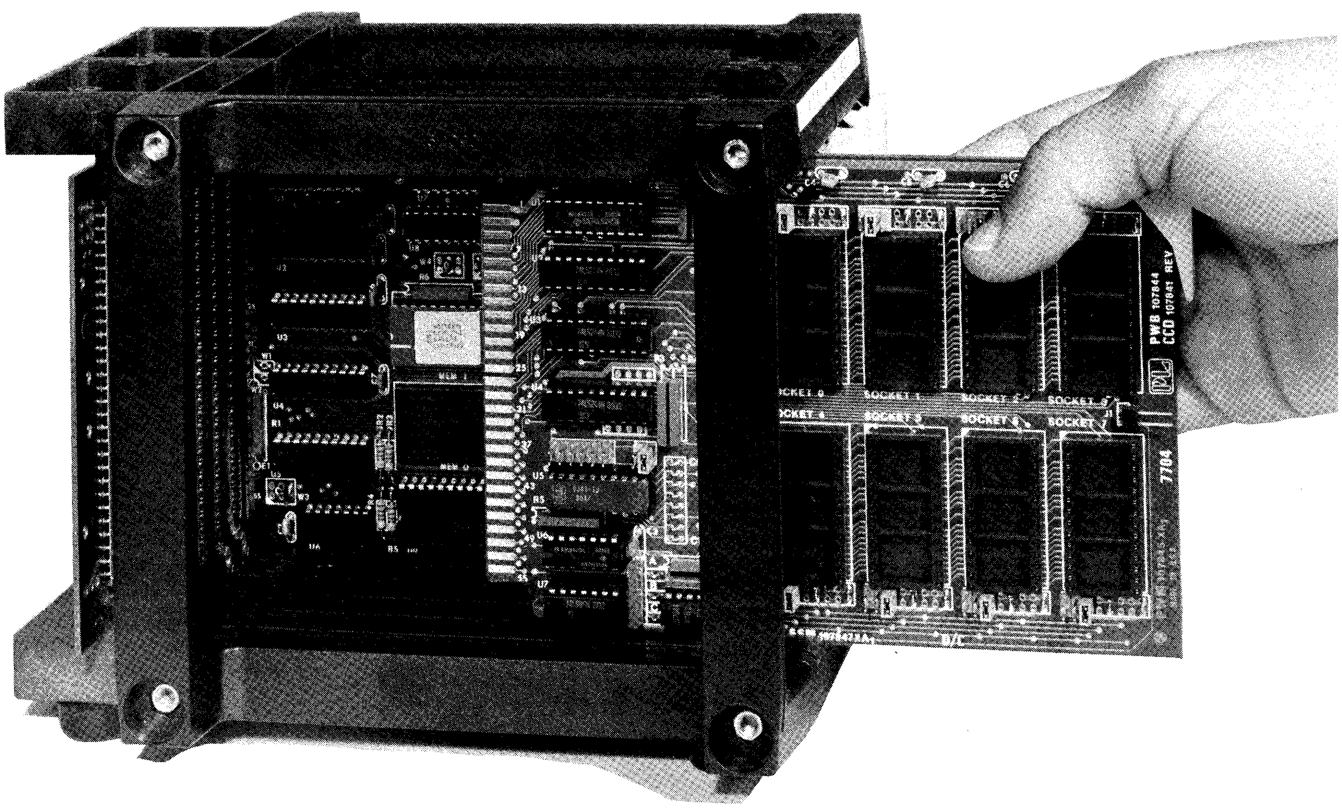


Figure 2-1. 7704 Installation

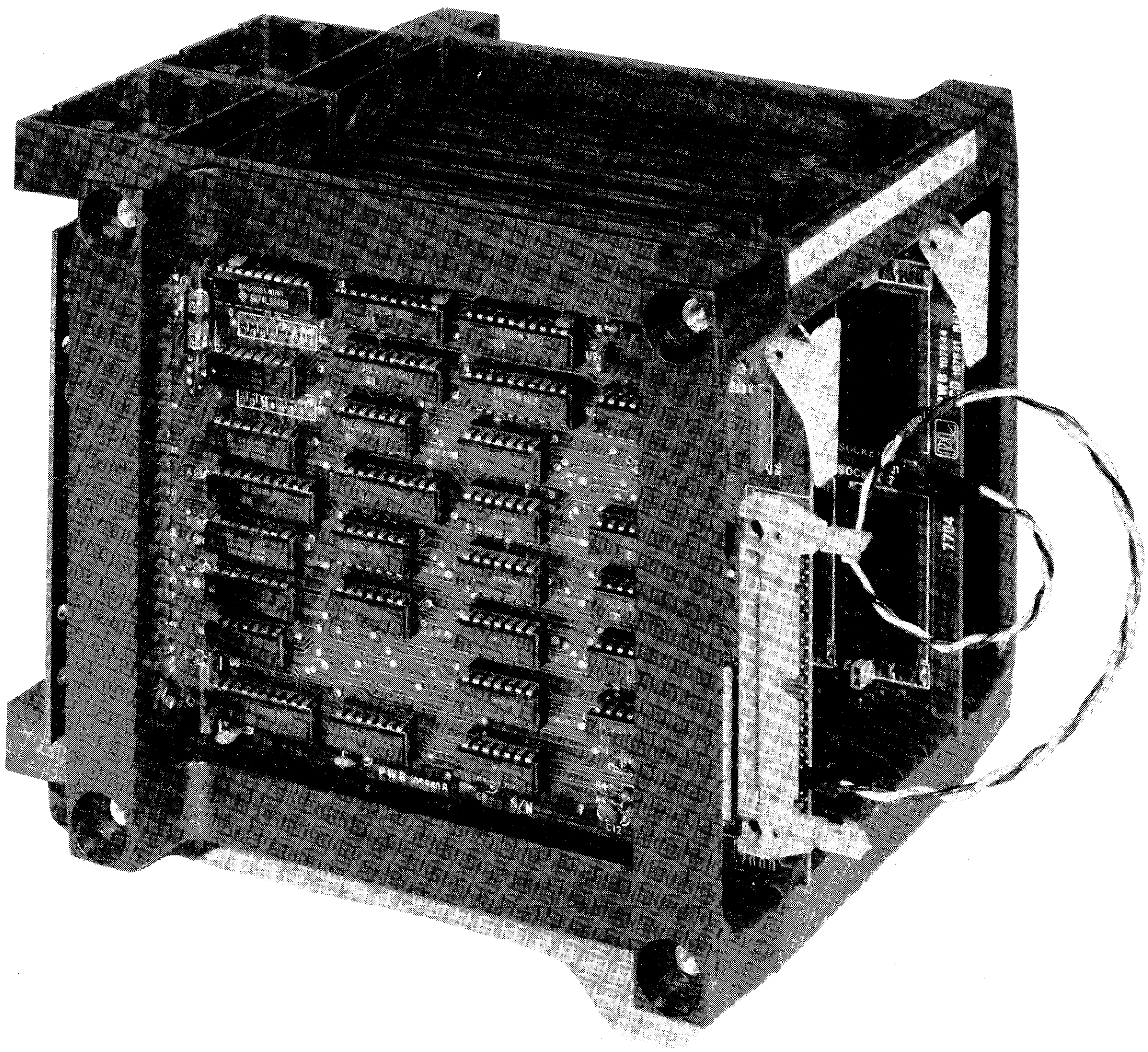


Figure 2-2. 7704 Segment Select Connector

WIRE JUMPERS

Some 7704 optional functions are selected by wire jumpers. When removing and replacing these jumpers, cut the jumper in half, then desolder and remove each half individually. Remaining solder should be removed, and new jumpers installed in the appropriate places. This procedure will prevent damage to circuit traces.

Most 7704 optional functions are selected by permanent 0.025 in. square posts which can be connected by slip on, slip off connectors. Part numbers for these connectors and headers are listed in Fig. 2-3. Figure 2-4 shows the location of these jumpers and some of the other features of the 7704.

Part	Manufacturer Part Number	
	Elco Corp.	Berg Electronics
2 Pin Header	00 8261 02 32 00 852	65611-102
4 Pin Header	00 8261 04 32 00 852	65611-104
6 Pin Header	00 8261 06 32 00 852	65611-106
8 Pin Header	00 8261 08 32 00 852	65611-108
Connector	00 8261 02 42 00 870	——

Figure 2-3. Part Numbers for 7704 Option Jumpers

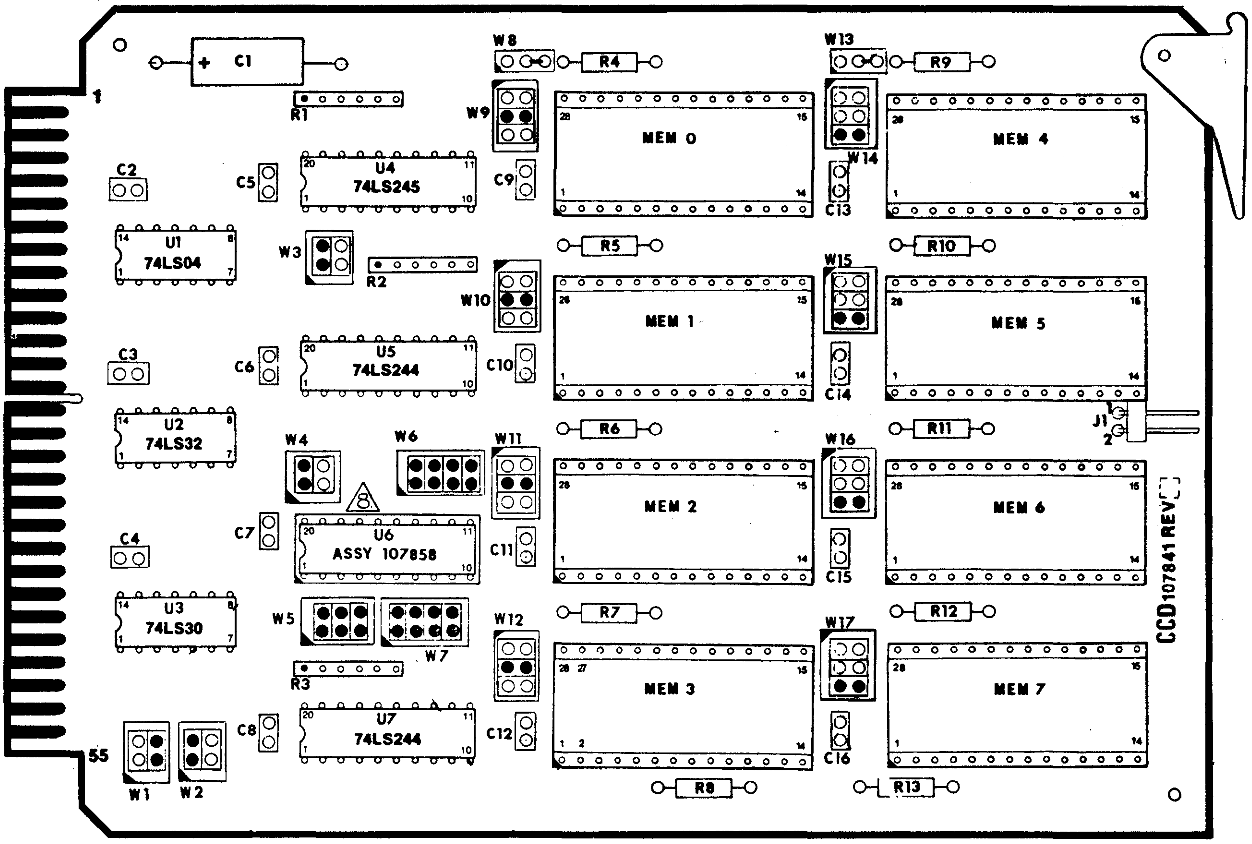


Figure 2-4. Physical Locations of Features on the 7704 Card

MEMORY DECODER

The eight memory sockets of the 7704 can accept any combiantion of 2K, 4K, and 8K ROMs and RAMs which conform to the specifications described in the Memory Type section. The combination of memory sizes and the address range each socket occupies are controlled by the Memory Decoder. The Memory Decoder contains 12 optional combinations, which are selected by jumper W4 1-2, 3-4, and jumpers W5, 1-2, 3-4, and 5-6. The physical locations of these jumpers can be found in Fig. 2-4. The 12 combinations and how to select them are shown in Fig. 2-5. Figures 2-6 through 2-21 are 64K memory maps which show the address field occupied by each socket for each option.

The Memory Decoder is a PROM. If other combinations of memory types or other address mapping is required, the PROM can be programmed with your own option. Two sections of the PROM have been left blank specifically for this purpose. The options contained in the Memory Decoder as shipped should suffice for most applicaitons. If other options are required, the writing of the program and the programming of the PROM would be the responsibility of the user.

Figure 2-5. Memory Decoder Options

OPTION	JUMPERS (X = JUMPER INSTALLED)					MEMORY PARTS BY SIZE			TOTAL MEMORY	ADDRESS RANGE	MEMORY PER SOCKET								COMMENTS
	W5			W4															
	5-6	3-4	1-2	1-2	3-4	8K	4K	2K			0	1	2	3	4	5	6	7	
As Shipped	X	X	X	X	—	0	4	4	24K	8000-DFFF	4	4	4	4	2	2	2	2	Standard as shipped from Pro-Log (4K, 2K mixed).
1	—	X	X	X	—	4	0	4	40K	0000-9FFF	8	8	8	8	2	2	2	2	8K, 2K mixed.
2	X	—	X	X	—	4	4	0	48K	0000-BFFF	8	8	8	8	4	4	4	4	8K, 2K mixed.
3	—	—	X	X	—	8	0	0	64K	0000-FFFF	8	8	8	8	8	8	8	8	All 8K.
4	X	X	—	X	—	0	0	8	16K	4000-7FFF	2	2	2	2	2	2	2	2	All 2K.
5	—	X	—	X	—	0	8	0	32K	8000-FFFF	4	4	4	4	4	4	4	4	All 4K.
6a	X	—	—	—	X*	4	0	0	32K	8000-FFFF	8	8	8	8	—	—	—	—	This option and option 6b go together. The MEMEX line is tied to decoder PROM input A8, so a low MEMEX state will select 6a, and a high will select 6b.
7	—	—	—	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Not programmed. Intentionally left blank for customer's own configuration.
8	X	X	X	—	—	0	4	4	24K	0000-5FFF	4	4	4	4	2	2	2	2	4K, 2K mixed; alternate standard.
9	—	X	X	—	—	0	1	7	18K	3800-7FFF	2	2	2	2	2	2	2	4	Use with 7804's standard configuration: three 4K ROM and one 2K RAM. Total memory on both cards is 32K. If all 4Ks are ROM and all 2Ks are RAM, you have 16K ROM and 16K RAM.
10	X	—	X	—	—	0	5	3	26K	1000-1FFF 2800-7FFF	4	2	2	2	4	4	4	4	Use with 7880 which has 4K ROM and 2K RAM. Option does not have consecutive addresses. Total memory for both cards is 32K. If all 4Ks are ROM and all 2Ks are RAM, you have 24K ROM and 8K RAM.
11	—	—	X	—	—	0	8	0	32K	0000-7FFF	4	4	4	4	4	4	4	4	All 4Ks. Like option 5 except occupies addresses 0000-7FFF.
12	X	X	—	—	—	0	0	8	16K	0000-3FFF	2	2	2	2	2	2	2	2	All 2Ks. Like option 4 except occupies addresses 0000-3FFF.
13	—	X	—	—	X**	0	8	0	32K	7FFF-0000	4	4	4	4	4	4	4	4	Test option for Pro-Log use only.
6b	X	—	—	—	X**	4	0	0	32K	8000-FFFF	—	—	—	—	8	8	8	8	Dual bank for 2764s; to work with option 6a using MEMEX high to select.
15	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Not programmed. Intentionally left blank for customer's owm configuration.

* Uses MEMEX with a low state at W4.
** Uses MEMEX with a high state at W4.

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X	← SOCKET 0 →															
1X	← SOCKET 1 →															
2X	← SOCKET 2 →															
3X	← SOCKET 3 →															
PAGE 4X	← SOCKET 4 →								← SOCKET 5 →							
5X	← SOCKET 6 →								← SOCKET 7 →							
6X																
7X																
PAGE 8X																
9X																
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-6. 7704 Option 0

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X	SOCKET 0															
1X	SOCKET 0															
2X	SOCKET 1															
3X	SOCKET 1															
PAGE 4X	SOCKET 2															
5X	SOCKET 2															
6X	SOCKET 3															
7X	SOCKET 3															
PAGE 8X	SOCKET 4								SOCKET 5							
9X	SOCKET 6								SOCKET 7							
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-7. 7704 Option 1

LSD / MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X	← SOCKET 0 →															
1X	← SOCKET 0 →															
2X	← SOCKET 1 →															
3X	← SOCKET 1 →															
PAGE 4X	← SOCKET 2 →															
5X	← SOCKET 2 →															
6X	← SOCKET 3 →															
7X	← SOCKET 3 →															
PAGE 8X	← SOCKET 4 →															
9X	← SOCKET 5 →															
AX	← SOCKET 6 →															
BX	← SOCKET 7 →															
PAGE CX																
DX																
EX																
FX																

Figure 2-8. 7704 Option 2

<table>
<tr><th>LSD / MSD</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>F</th></tr>
<tr><td>PAGE 0X</td><td colspan="16">SOCKET 0</td></tr>
<tr><td>1X</td><td colspan="16">SOCKET 0</td></tr>
<tr><td>2X</td><td colspan="16">SOCKET 1</td></tr>
<tr><td>3X</td><td colspan="16">SOCKET 1</td></tr>
<tr><td>PAGE 4X</td><td colspan="16">SOCKET 2</td></tr>
<tr><td>5X</td><td colspan="16">SOCKET 2</td></tr>
<tr><td>6X</td><td colspan="16">SOCKET 3</td></tr>
<tr><td>7X</td><td colspan="16">SOCKET 3</td></tr>
<tr><td>PAGE 8X</td><td colspan="16">SOCKET 4</td></tr>
<tr><td>9X</td><td colspan="16">SOCKET 4</td></tr>
<tr><td>AX</td><td colspan="16">SOCKET 5</td></tr>
<tr><td>BX</td><td colspan="16">SOCKET 5</td></tr>
<tr><td>PAGE CX</td><td colspan="16">SOCKET 6</td></tr>
<tr><td>DX</td><td colspan="16">SOCKET 6</td></tr>
<tr><td>EX</td><td colspan="16">SOCKET 7</td></tr>
<tr><td>FX</td><td colspan="16">SOCKET 7</td></tr>
</table>

Figure 2-9. 7704 Option 3

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X																
1X																
2X																
3X																
PAGE 4X	◄— SOCKET 0 —►								◄— SOCKET 1 —►							
5X	◄— SOCKET 2 —►								◄— SOCKET 3 —►							
6X	◄— SOCKET 4 —►								◄— SOCKET 5 —►							
7X	◄— SOCKET 6 —►								◄— SOCKET 7 —►							
PAGE 8X																
9X																
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-10. 7704 Option 4

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X																
1X																
2X																
3X																
PAGE 4X																
5X																
6X																
7X																
PAGE 8X	← SOCKET 0 →															
9X	← SOCKET 1 →															
AX	← SOCKET 2 →															
BX	← SOCKET 3 →															
PAGE CX	← SOCKET 4 →															
DX	← SOCKET 5 →															
EX	← SOCKET 6 →															
FX	← SOCKET 7 →															

Figure 2-11. Option 5

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X	← SOCKET 0 →															
1X	← SOCKET 0 →															
2X	← SOCKET 1 →															
3X	← SOCKET 1 →															
PAGE 4X	← SOCKET 2 →															
5X	← SOCKET 2 →															
6X	← SOCKET 3 →															
7X	← SOCKET 3 →															
PAGE 8X																
9X																
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-12. 7704 Option 6a

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X																
1X																
2X																
3X																
PAGE 4X																
5X																
6X																
7X																
PAGE 8X																
9X																
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-13. 7704 Option 7

LSD / MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X																
1X																
2X																
3X																
PAGE 4X																
5X																
6X																
7X																
PAGE 8X	← SOCKET 0 →															
9X	← SOCKET 1 →															
AX	← SOCKET 2 →															
BX	← SOCKET 3 →															
PAGE CX	← SOCKET 4 →								← SOCKET 5 →							
DX	← SOCKET 6 →								← SOCKET 7 →							
EX																
FX																

Figure 2-14. 7704 Option 8

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<tr><td>1X</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>2X</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>3X</td><td colspan="8"></td><td colspan="8">SOCKET 0</td></tr>
<tr><td>PAGE 4X</td><td colspan="8">SOCKET 1</td><td colspan="8">SOCKET 2</td></tr>
<tr><td>5X</td><td colspan="8">SOCKET 3</td><td colspan="8">SOCKET 4</td></tr>
<tr><td>6X</td><td colspan="8">SOCKET 5</td><td colspan="8">SOCKET 6</td></tr>
<tr><td>7X</td><td colspan="16">SOCKET 7</td></tr>
<tr><td>PAGE 8X</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>9X</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>AX</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>BX</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>PAGE CX</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>DX</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>EX</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>FX</td><td colspan="8"></td><td colspan="8"></td></tr>
</table>

Figure 2-15. 7704 Option 9

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X																
1X	← SOCKET 0 →															
2X									← SOCKET 1 →							
3X	← SOCKET 2 →								← SOCKET 3 →							
PAGE 4X	← SOCKET 4 →															
5X	← SOCKET 5 →															
6X	← SOCKET 6 →															
7X	← SOCKET 7 →															
PAGE 8X																
9X																
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-16. 7704 Option 10

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X	← SOCKET 0 →															
1X	← SOCKET 1 →															
2X	← SOCKET 2 →															
3X	← SOCKET 3 →															
PAGE 4X	← SOCKET 4 →															
5X	← SOCKET 5 →															
6X	← SOCKET 6 →															
7X	← SOCKET 7 →															
PAGE 8X																
9X																
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-17. 7704 Option 11

LSD / MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X	← SOCKET 0 →								← SOCKET 1 →							
1X	← SOCKET 2 →								← SOCKET 3 →							
2X	← SOCKET 4 →								← SOCKET 5 →							
3X	← SOCKET 6 →								← SOCKET 7 →							
PAGE 4X																
5X																
6X																
7X																
PAGE 8X																
9X																
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-18. 7704 Option 12

LSD / MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X	← SOCKET 7 →															
1X	← SOCKET 6 →															
2X	← SOCKET 5 →															
3X	← SOCKET 4 →															
PAGE 4X	← SOCKET 3 →															
5X	← SOCKET 2 →															
6X	← SOCKET 1 →															
7X	← SOCKET 0 →															
PAGE 8X																
9X																
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-19. 7704 Option 13

LSD / MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X																
1X																
2X																
3X																
PAGE 4X																
5X																
6X																
7X																
PAGE 8X	← SOCKET 4 →															
9X	← SOCKET 4 →															
AX	← SOCKET 5 →															
BX	← SOCKET 5 →															
PAGE CX	← SOCKET 6 →															
DX	← SOCKET 6 →															
EX	← SOCKET 7 →															
FX	← SOCKET 7 →															

Figure 2-20. 7704 Option 6b

LSD / MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PAGE 0X																
1X																
2X																
3X																
PAGE 4X																
5X																
6X																
7X																
PAGE 8X																
9X																
AX																
BX																
PAGE CX																
DX																
EX																
FX																

Figure 2-21. 7704 Option 15

MEMORY TYPE

The 7704 uses six kinds of memory: 2K, 4K, and 8K ROMs and RAMs. The eight memory sockets are designed to accept memory components compatible with the JEDEC 28 pin standard pinout. Each socket can be individually configured for the 2K RAMs or any of the ROMs. The 4K and 8K RAMs are the exception. The sockets can only be configured for these in groups of four. The groups will consist either of sockets 0, 1, 2, and 3, or sockets 4, 5, 6, and 7.

After having chosen the memory combination best suited to your needs, as discussed in the Memory Decoder section, the sockets should be configured accordingly. Figure 2-22 shows where to place the memory socket jumpers for each kind of memory. The location of these jumpers is shown in Fig. 2-4. Jumpers W9, W10, W11, W12, W14, W15, W16 and W17 correspond to sockets 0 through 7 respectively. Jumpers W8 and W13 are used to configure the sockets for 4K or 8K RAMs. Jumper W8 affects sockets 0, 1, 2, and 3, jumper W13 affects sockets 4, 5, 6, and 7.

Figure 2-23 is a list of pin compatible memory components for use on the 7704 card. The recommended memory components are indicated by an asterisk. If you wish to use another memory component, compare its data sheet to the socket configurations. Also, check the data sheet for any special requirements, and be sure the parts are fast enough for the processor you will be using.

Note: As of this writing, 4K and 8K byte-wide RAMs are not available and have not been tested on the 7704. Any 4K or 8K byte-wide RAM that conforms to the JEDEC 28 pin standard and is fully static should be able to be used on the 7704. Pro-Log will be evaluating some of these parts as they become available.

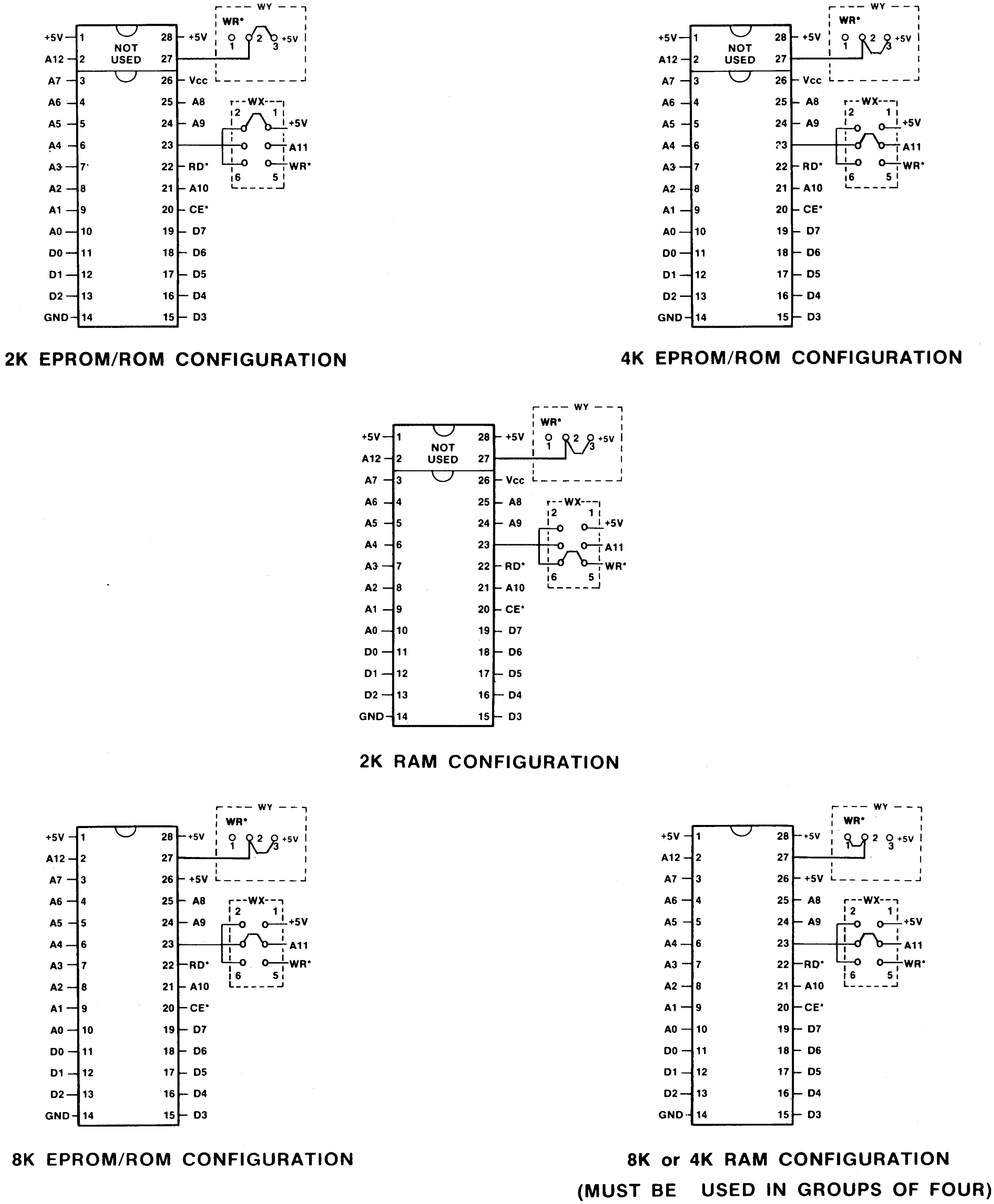


Figure 2-22. Socket Configurations

CHIP #	ORGANIZATION	ACCESS
INTEL CORPORATION		
218122K	2K SRAM	150
2716*	2K EPROM	350-650
2732*	4K EPROM	450-550
2732A*	4K EPROM	200-250
2764*	8K EPROM	200-250
MOSTEK CORPORATION		
MK34000	2K ROM	350
MK37000	8K ROM	300
MK2716*	2K EPROM	300
MK2764*	8K EPROM	450
MK4802	2K SRAM	
NATIONAL SEMICONDUCTOR		
MM2716*	2K EPROM	350-450
MOTOROLA		
MCM2716*	2K EPROM	250-450
TEXAS INSTRUMENTS		
TMS2516*	2K EPROM	
MITSUBISHI		
M58725*	2K SRAM	200
NEC MICROCOMPUTERS		
uPD2716*	2K EPROM	450
uPD2732*	4K EPROM	no spec
AMERICAN MICROSYSTEMS (AMI)		
S4028	2K SRAM	200
SYNERTEK		
SY2716*	2K EPROM	350-450
OKI		
MSM5128*	2K SRAM	150-200-250
TOSHIBA		
TMM2016*	2K SRAM	150-250

*Recommended Devices

Figure 2-23. Memory Components List

UNUSED SOCKETS

Aside from different memory types that can be used and the different combinations that can be selected, further tailoring can be done to suit the 7704 card to your application. This can be done by disabling any unused sockets.

Jumpers W7, 1-2 through 7-8, and W6, 7-8 through 1-2, correspond to sockets 0-7 respectively.

When a socket is disabled, the chip select signal is disconnected from the socket. Also the data bus buffer no longer responds to memory requests in the address range of the unused socket. This means that memory on other cards in the system can occupy this address space, without interference from the 7704 card.

Any number and combination of sockets may be disabled. By this method, the 7704 card can be configured to occupy as little as 2K of memory space. These 2K blocks may occupy adjacent address fields or be widely separated. They may be mapped anywhere within a 64K memory system on the natural 2K boundaries.

MEMEX

The function and operation of the MEMEX will be explained in Section 3. This section is to explain the jumper options affecting MEMEX.

On the 7704 card, MEMEX can be used in one of two ways. The first method is to use the MEMEX line to enable the card. Using this method, two 7704's can occupy the same address field, only one of which is enabled at a time depending on the logic state of the MEMEX line. The second method seperates the memory on the 7704 into two banks. Only one half of the card is enabled at a time. Therefore, both halves can occupy the same address field.

As shipped, the card employs the first method. The 7704 card is enabled when MEMEX is low. To reverse its polarity, remove jumper W2 from position 1-2 and replace it with one at position 3-4. The location of this jumper is shown in Fig. 2-4. When using two of these cards which are both going to occupy the same address field, one must have its polarity changed.

It is important to ensure that the MEMEX line is not left floating. The line must be either controlled by some other card in the system, or tied to ground on the 7704 itself. Pro-Log processor cards either control the MEMEX line or simply tie it to ground. If there is no card in the system controlling MEMEX, or if you want the card to disregard MEMEX, jumper W1 can be removed from position 3-4 and be replaced by one at position 1-2. This will tie the line to ground and permanently enable the card.

If MEMEX will be used to divide the 7704 into two banks, jumper W1 should be in position 1-2 to permanently enable the card. Also, jumper W4 should be in position 3-4.

Jumper W4 serves two purposes. It is part of the Memory Decoder Control jumpers. A jumper in position 1-2 serves as a low level input to the Memory Decoder. With no jumper installed it is a high level input. A jumper in position 3-4 connects the MEMEX line to the Memory Decoder input. Therefore, by changing the state of the MEMEX line, you can select a different Memory Decoder option. This is not something you would want to do with most of the options. However, with options 6A and 6B it can be done. Option 6A only uses sockets 0-3. Option 6B only uses sockets 4-7. Both options use the same memory address field. Therefore, by controlling the MEMEX line, you can select one of two memory banks on the 7704 card.

Segment Select

The function and operation of the Segment Select line will be explained in Section 3. This section is to explain the jumper options affecting Segment Select.

The Segment Select line is not a part of the STD BUS. It is an external line which must be connected on the card ejector side of the 7704, when it is used. Figure 2-2, shows the location of the connector.

The connector type is a 2-pin 0.1 inch center connector. The cable should be a twisted pair, consisting of one signal line and one ground line for added noise immunity. Figure 2-26 shows which pin is signal and which is ground.

An I/O card, such as Pro-Log's 7605 card, along with an RC704 cable can be used to control the line. One output bit, or line, per 7704 card is required. Therefore, one output port can control eight 7704 cards.

As shipped the card is enabled when the Segment Select line is in the high state. Its polarity can be reversed by removing jumper W3 from position 1-2 and replacing it with one at position 3-4. See Fig. 2-4.

With jumper W3 in position 1-2, the Segment Select line can be left unconnected. A pull-up resistor on the line will hold it in the active condition. If jumper W3 is in position 3-4 however, the line must be controlled in some manner, or the card will remain permanently disabled.

Specifications

Figures 2-24 and 2-25 are electrical and environmental specifications. Figures 2-26 and 2-27 describe the specifications for the interface connections and card edge connections.
Figures 2-28 through 2-33 are the timing requirements necessary for the 7704.

Recommended Operating Limits					Absolute Non-Operating Limits		
Mnem.	Parameter	Min.	Typ.	Max.	Min.	Max.	Units
Vcc	Supply Voltage	4.65	5.00	5.35	0	7.00	Volts
—	Free Air Temp.	0	+25	+55	-40	+75	°C
—	Non-Condensing Relative Humidity	5		95	5	95	%RH

Figure 2-24. Electrical and Environmental Specifications

Mnem.	Parameter	Min.	Typ.	Max	Units
Icc	Vcc Supply Current			500*	MilliAmp

*With memory sockets empty

Figure 2-25. Electrical Characteristics

MNEMONIC	INPUT (LSTTL LOADS)	OUTPUT (LSTTL DRIVE)	PIN NUMBER	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
SEGMENT 0*	5		2	1	GND		GROUND

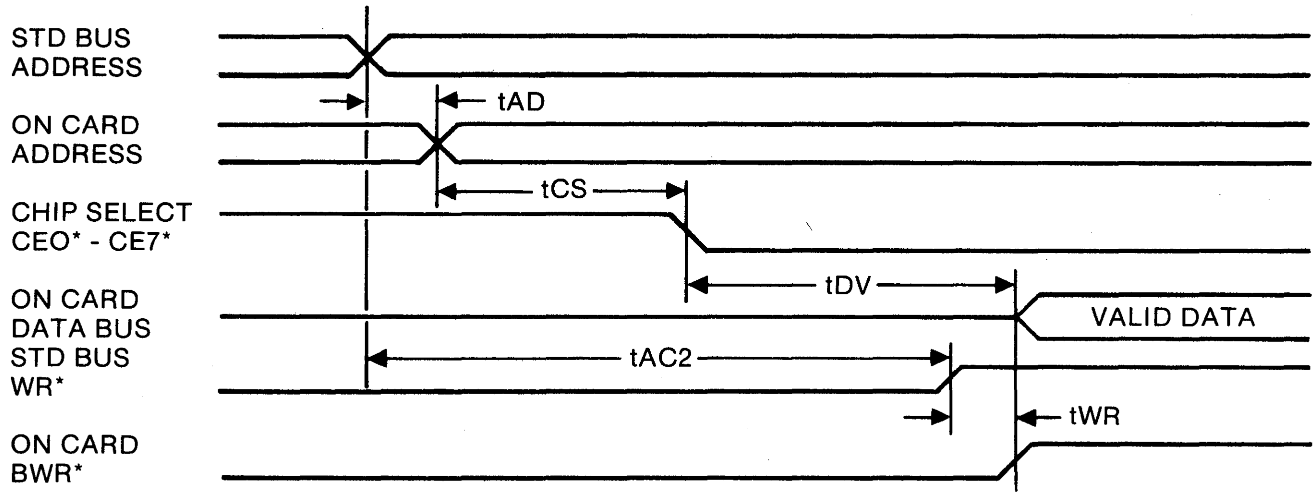
*Active low-level logic

Figure 2-26. Interface Specifications

MNEMONIC	INPUT (LSTTL LOADS)	OUTPUT (LSTTL DRIVE)	PIN NUMBER	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15	1		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	1		22	21		1	A4
A11	1		24	13		1	A3
A10	1		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*	1		34	33			IORQ*
MEMEX*	1		36	35			IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PC1	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic

Figure 2-27. Edge Connector Pin List



SYMBOL	PARAMETER	NANOSECONDS MIN.	TYP.	MAX.
tAC	7704 minimum safe write cycle time	220		
tAD	Addreses buffer delay time (STD Bus to memory socket)		18	30
tCS	Chip select logic time (STD Bus to memory socket)		45	70
tDV	Chip select to data valid time (STD Bus to memory socket)		74	112
tWR	Write buffer delay (STD Bus to memory socket)		12	18

All above times are assuming that WR*, MEMRQ*, MEMEX and SEGMENT are true prior to STD BUS address becoming true.

A memory device with an access time equal to tDV was used here. A memory device faster than tDV will not improve the access time of the card.

To find write access time of the 7704 with a specific memory device of longer than 112 nsec access time use the following equations.

$$tWA = tAC - tDV + tAA$$
$$tWA \geq tAC$$

Where: tWA = Total access time of card and memory device for write.

tAC = 7704 minimum safe write cycle time.

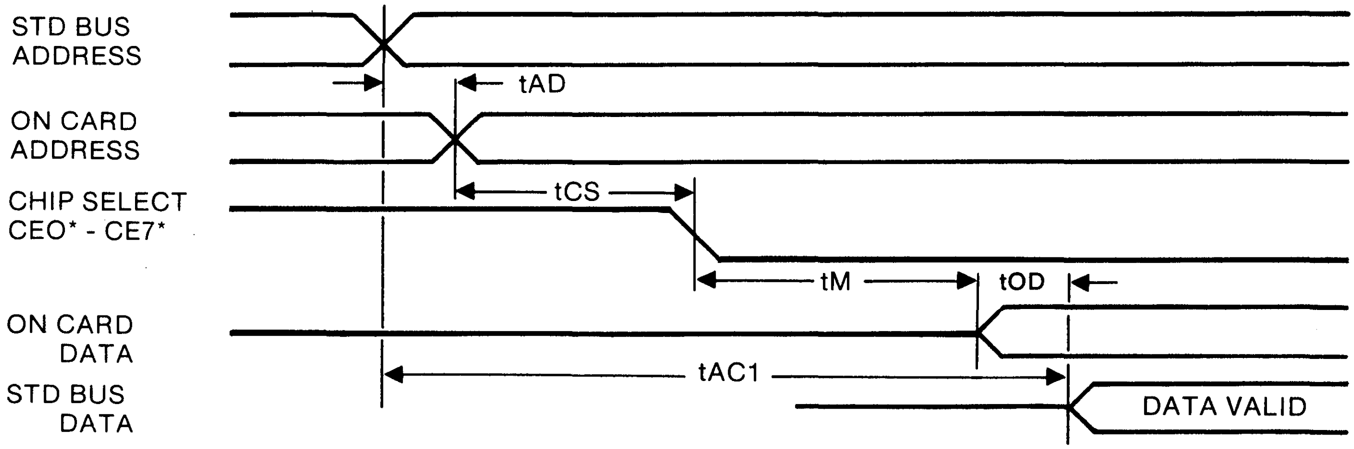
tDV = 7704 chip select till data valid at memory chips.

tAA = Memory device access time.

If device access time (tAA) is less than or equal to 112 nsec then tAC is the total access time (200 nsec).

* LOW LEVEL ACTIVE

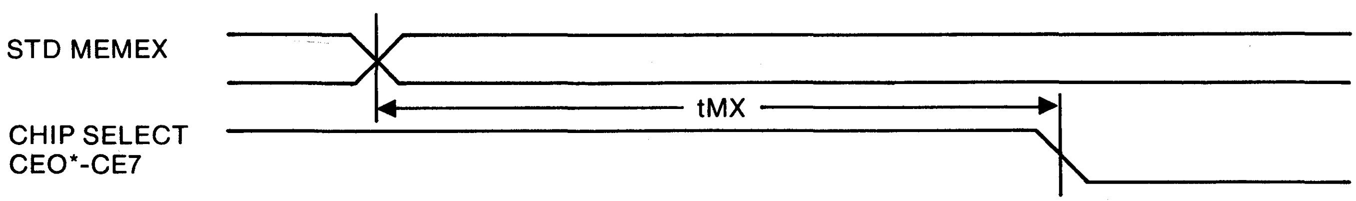
Figure 2-28. 7704 Timing for Write



SYMBOL	PARAMETER	NANOSECONDS		
		MIN	TYP	MAX
tAC	Minimum safe access time for read	220		
tAD	Address buffer time delay		18	30
tCS	Chip select logic time		45	70
tOD	Data bus buffer time delay		8	12
tM	Data buffer enable time		64	100

All above times are assuming that RD*, MEMRQ*, MEMEX and SEGMENT are active prior to STD BUS address becoming true.

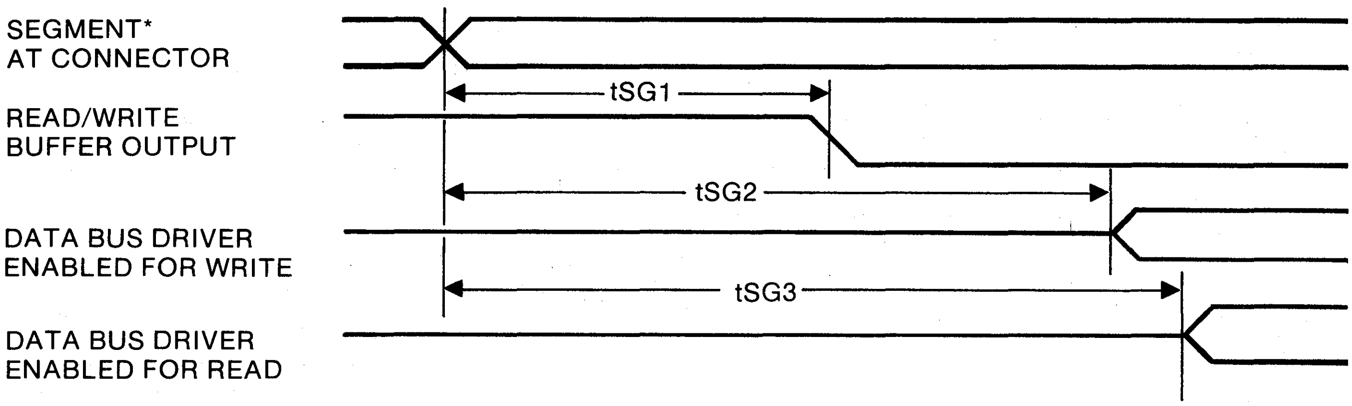
Figure 2-29. 7704 Timing for Read



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
TMX	Time MEMEX valid to chip select*	77	118

The above parameter true if all other signals are active prior to MEMEX going active.

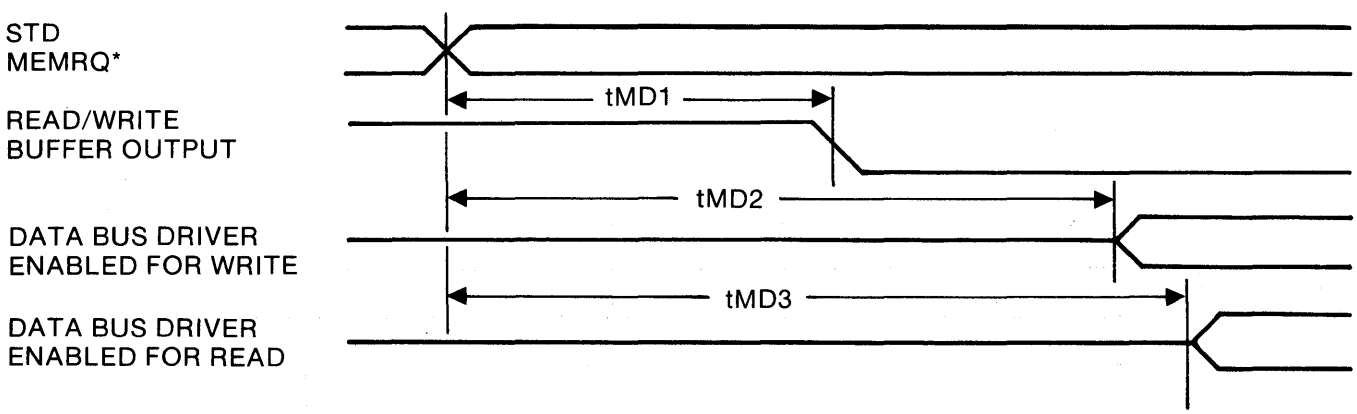
Figure 2-30. 7704 MEMEX Timing



SYMBOL	PARAMETER	NANOSECONDS TYP	MAX
tSG1	SEGMENT* valid to RD* + WR* buffer output valid	54	82
tSG2	SEGMENT* valid to data bus driver enabled for write	75	114
tSG3	SEGMENT* valid to data bus driver enabled for read	81	122

The above parameters are true if all other signals are active prior to Segment* going active.

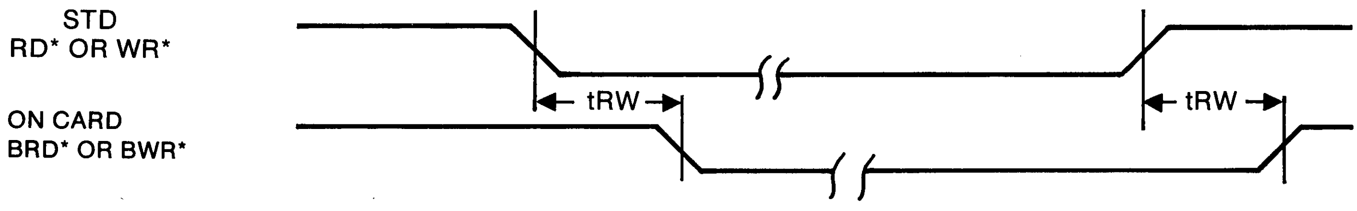
Figure 2-31. 7704 Segments Timing



SYMBOL	PARAMETER	NANOSECONDS TYP	MAX
tMD1	Time MEMRQ* to RD* + WR* buffer enabled	46	70
tMD2	Time MEMRQ* to data bus driver enabled for write	67	102
tMD3	Time MEMRQ* to data bus driver enabled for read	73	110

Above parameters valid if all other signals are active prior to MEMRQ* going active.

Figure 2-32. 7704 Segments MEMRQ*



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tRW	Time RD* or WR* till BRD* or BWR* on 7704 card	12	**18**

Above parameter valid if all other signals are active prior to RD* or WR* changing state.

Figure 2-33. 7704 RD* or WR* Timing

Operation and Programming

This section describes the functions and use of the 7704 card. The card is designed to be a versatile part of your memory system.

It can be used in both small and large scale applications. By using the memory size and mapping options described in Section 2 and the MEMEX and Segment Select lines described in this section, the 7704 can fill the memory requirements of virtually any system.

MEMEX

The MEMEX line is a part of the STD BUS. It is used as a memory bank select line. Using this line allows two banks of memory to occupy the same address field. Only one of the banks is selected at a time, depending on the logic state of the MEMEX line.

It is normally controlled by a memory segment controller, or an output port. The segment controller or output port can be either on the processor card, or on some other card in the system. Some Pro-Log processor cards have an onboard output port for controlling MEMEX.

MEMEX Example

An example of how MEMEX can be used is shown in Fig. 3-1. It shows a 124K memory system. It is comprised of 4K of RAM and 120K of ROM. The RAM is on the processor card and is permanently enabled. That is, it ignores MEMEX. The ROM is in two 60K banks, one bank on each 7704 card. Only one card is enabled at a time dash the one on the left when MEMEX is low, and the one on the right when it is high.

At power up, the MEMEX port is low. The Primary memory bank is therefore enabled. The processor can then choose Primary or Expanded memory simply by manipulating the MEMEX line.

A second example is shown in Fig. 3-2. In this example the two memory banks both reside on one 7704 card. The system has 96K of memory, consisting of 64K ROM and 32K RAM. The 64K ROM is in two banks of 32K each. The RAM is on two 16K RAM cards, and is permanently enabled.

At power up, the MEMEX port is low. Primary memory is therefore enabled. Again, the processor can choose between Primary and Expanded memory simply by manipulating the MEMEX line.

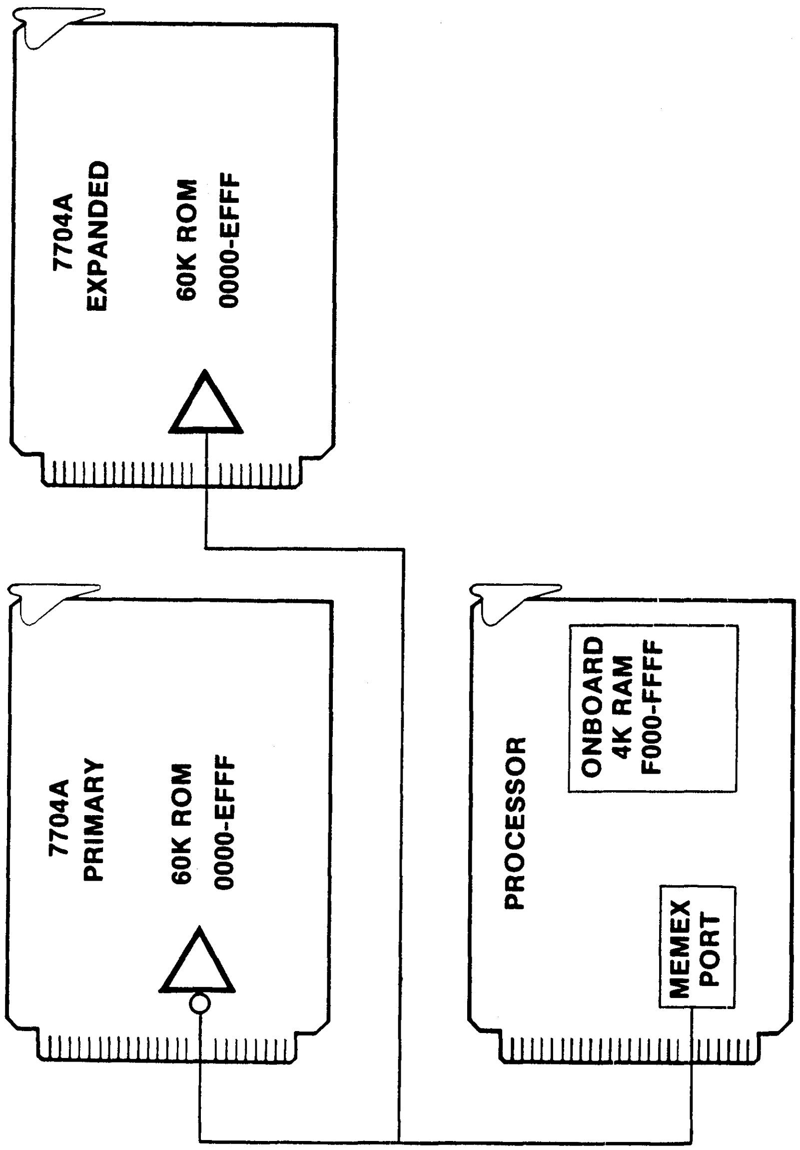


Figure 3-1. 7704 MEMEX Example

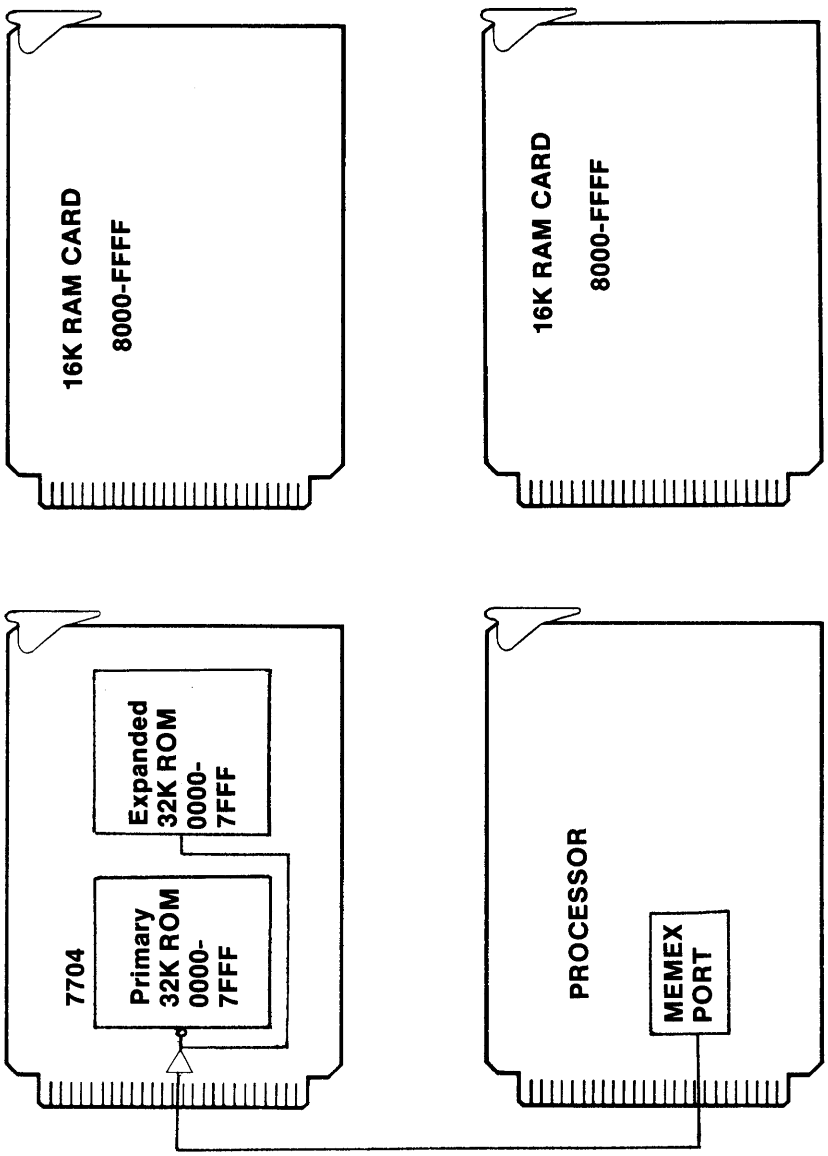


Figure 3-2. 7704 MEMEX Example

MEMEX Control Software

The software for controlling MEMEX requires some special consideration. Care must be taken to avoid confusion when changing memory banks.

There are a number of ways to deal with this. What follows are a few examples.

MEMEX Control Software Example One

In many systems using MEMEX, it will be advantageous to keep some section of memory permanently enabled, a section which disregards MEMEX. This may be a section of ROM memory at the low order addresses, or a section of RAM used to store registers, program variables, and the stack, or a section of ROM containing interrupt service routines that need to be quickly accessible at all times.

If your system will have a permanently enabled section of memory, the MEMEX Control software can reside in this section. If the section is ROM, the program would simply reside in the ROM. If the section is RAM, the processor could load the program into the RAM. The program would be stored in ROM, disc, or some other nonvolatile memory. The processor would load the program into RAM as part of the power-up intialization process.

Using the system in Fig. 3-1 as a model, a program could be written like the one shown in Fig. 3-3. It assumes you are jumping from a main program in one bank to a subroutine in the other bank. The address of the subroutine you are jumping to must be in the HL register pair. The program selects the proper memory bank and jumps to the subroutine. When the subroutine is exited, the processor returns to the MEMEX control program. The program reselects the original bank, then returns to the program from which it came.

Fig. 3-3 shows two programs. One to jump to a subroutine in Expanded memory, and one to jump to a subroutine in Primary memory.

HEXADECIMAL			MNEMONIC			TITLE MEMEX SOFTWARE Ex 1 DATE	
PAGE ADR	LINE ADR	INSTR.	LABEL	INSTR.	MODIFIER		COMMENTS
FF	E 0	3E	(TO EXP)	LDAI			SET MEMEX HIGH, ENABLES
	1	01		—	01		EXPANDED MEMORY
	2	D3		OPA			
	3	XX		—	XX		← PORT ADDRESS
	4	E5		PSP	HL		PUSH RETURN ADDRESS (FFEA)
	5	21		LDPI	HL	P	ON TO STACK
	6	EA		—		E	
	7	EF		—		R	
	8	E3		XCPT	HL	M	
	9	E9		JPN		A	JUMP TO SUBROUTINE AT H,L
	A	3E		LDAI		N	SET MEMEX LOW ENABLES
	B	00		—	00	E	PRIMARY MEMORY
	C	D3		OPA		N	
	D	XX		—	XX	T	← PORT ADDRESS
	E	C9		RTS			EXIT
	F					M	
	F 0	3E	(TO PRI)	LDAI		E	SET MEMEX LOW ENABLES
	1	00		—	00	M	PRIMARY MEMORY
	2	D3		OPA		O	
	3	XX		—		R	PORT ADDRESS
	4	E5		PSP	HL	Y	PUSH RETURN ADDRESS (FFFA)
	5	21		LDPI	HL		ONTO STACK
	6	FA		—			
	7	EF					
	8	E3		XCPT	HL		
	9	E9		JPN	HL		JUMP TO SUBROUTINE AT HL
	A	3E		LDAI			SET MEMEX HIGH. ENABLES
	B	01		—			EXPANDED MEMORY
	C	D3		OPA			
	D	XX		—	XX		← PORT ADDRESS
	E	C9		RTS			EXIT
	F						

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Figure 3-3. 7704 MEMEX Software Example One

MEMEX Control Software Example Two

In the first example it was assumed that anytime the program jumped from one bank to the other it was to jump to a subroutine. Fig. 3-4 is a program for jumping from one bank to the other, but not as a subroutine.

The program simply changes the state of the MEMEX line, and then jumps to the address in the HL register pair. Again the program is divided up into two sections dash one to go from Primary to Expanded memory, and one to do the opposite.

TITLE MEMEX SOFTWARE EX2. DATE

HEXADECIMAL PAGE ADR	LINE ADR	INSTR.	MNEMONIC LABEL	INSTR.	MODIFIER	COMMENTS
FF	F 0	3E	TO EXP	LDAI		PERMANENT MEMORY — SET MEMEX HIGH SELECT EXPANDED
	1	01		—		MEMORY
	2	D3		OPA		
	3	XX		—		PORT ADDRESS
	4	E9		JPN	H,L	JUMP TO ADDRESS IN H,L
	5					
	6					
	7					
	8					
	9	3E	TO PRI	LDAI		SET MEMEX LOW SELECT PRIMARY
	A	00		—		MEMORY
	B	D3		OPA		
	C	XX		—		PORT ADDRESS
	D	E9		JPN	HL	JUMP TO ADDRESS IN H,L PAIR.
	E					
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

Figure 3-4 7704. MEMEX Software Example Two

MEMEX Control Software Example Three

So far we have looked at MEMEX control software residing in a section of memory which is permanently enabled. Figures 3-5 and 3-6 show how the control software can reside in memory that is affected by MEMEX.

Figure 3-5 shows how a program can be written to jump from a program in Primary memory to a subroutine in Expanded memory. Note that both sections of the program reside at the same addresses. However, one part is in Primary memory and one part is in Expanded memory.

Figure 3-6 shows how the program looks to the processor. When it is run, it becomes one coherent program.

This program only allows for jumping from Primary memory to a subroutine in Expanded memory and then returning. In normal operation you would probably also want one to do the opposite.

To use the program, you must be in Primary memory. When you want to jump to a subroutine in Expanded memory, you load the address of the subroutine into the HL register pair. Then perform a Jump to Subroutine to the MEMEX control program. The program will direct the processor to change memory banks and jump to the subroutine. After running the subroutine, the processor will return to your original program.

TITLE MEMEX SOFTWARE EX. 3 DATE

HEXADECIMAL PAGE ADR	LINE ADR	INSTR.	LABEL	MNEMONIC INSTR.	MODIFIER		COMMENTS
FF	F0	3E		LDAI			JUMP TO EXPAND MEMORY
	1	01		—	01	P	
	2	D3		OPA		R	
	3	XX		—		I	← PORT ADDRESS
	4	00		NOP		M	UNUSED
	5	00		NOP		A	
	6	00		NOP		R	
	7	00		NOP		Y	
	8	00		NOP			
	9	00		NOP		M	
	A	00		NOP		E	
	B	00		NOP		M	
	C	00		NOP		O	
	D	00		NOP		RY	
	E	C9		RTS			EXIT
	F						
FF	F0	00		NOP			UNUSED
	1	00		NOP		E	
	2	00		NOP		X	
	3	00		NOP		P	
	4	E5		PSP	HL	A	PUSH RETURN ADDRESS (EFFA)
	5	21		LDPI	HL	N	ONTO STACK
	6	FA		—		D	
	7	EF		—		E	
	8	E3		XCPT	HL	D	
	9	E9		JPN	HL		JUMP TO SUBROUTINE AT H & L
	A	3E		LDAI		M	JUMP TO PRIMARY MEMORY
	B	00		—	00	E	
	C	D3		OPA		M	
	D	XX		—		O	← PORT ADDRESS
	E	00		NOP		RY	UNUSED
	F						

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Figure 3-5. 7704 MEMEX Software Example Three

HEXADECIMAL PAGE ADR	LINE ADR	INSTR.	MNEMONIC LABEL	INSTR.	MODIFIER	TITLE RUNNING EX3 DATE — COMMENTS
FF	F 0	3E		LDAI		JUMP TO EXPAND MEMORY
	1	01		-	01	
	2	D3		OPA		
	3	XX		—		← PORT ADDRESS
	4	E5		PSP	HL	PUSH RETURN ADDRESS ONTO STACK (FEFA)
	5	21		LDPI	HL	
	6	FA		—		
	7	FF		—		
	8	E3		XCPT	HL	
	9	E9		JPN	HL	JUMP TO SUBROUTINE AT H,L
	A	3E		LDAI		JUMP TO PRIMARY MEMORY
	B	00		—	00	
	C	D3		OPA		
	D	XX		—		← PORT ADDRESS
	E	C9		RTS		EXIT
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

Figure 3-6. 7704 Running Example Three

MEMEX Control Software Example Four

The example shown in Fig. 3-7 is similar to the last example. In this one however, rather than jumping from one bank to another as a subroutine, this program performs a simple jump.

This program is in two sections. One to go from Primary to Expanded memory, and one to do the opposite.

Fig. 3-8 shows how the programs looks to the processor. To the processor, either program appears to be one coherent program.

To use the program, load the address of the program you want to jump to into the HL register pair. Then jump to the MEMEX control program. The processor is directed to change memory banks, then jump to the program you requested.

TITLE MEMEX SOFTWARE EX4. DATE

PAGE ADR	LINE ADR	INSTR.	LABEL	INSTR.	MODIFIER		COMMENTS
FF	F0	0E	TO EXP	LDAI		PRIMARY MEMORY	JUMP TO EXPANDED MEMORY
	1	01		—	01		
	2	D3		OPA			
	3	XX		—			← PORT ADDRESS
	4	00		NOP			UNUSED
	5						
	6						
	7						
	8	00	TO PRI	NOP			UNUSED
	9	00		NOP			
	A	00		NOP			
	B	00		NOP			
	C	E9		JPN	HL		JUMP TO ADDRESS IN H,L
	D						
	E						
	F						
FF	F0	00	TO EXP	NOP		EXPANDED MEMORY	UNUSED
	1	00		NOP			
	2	00		NOP			
	3	00		NOP			
	4	E9		JPN	HL		JUMP TO ADDRESS IN H,L
	5						
	6						
	7						
	8	3E	TO PRI	LDAI			JUMP TO PRIMARY MEMORY
	9	00		—	00		
	A	D3		OPA			
	B	XX		—			← PORT ADDRESS
	C	00		NOP			UNUSED
	D						
	E						
	F						

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Figure 3-7. 7704 MEMEX Software Example Four

TITLE RUNNING EX4 DATE

PAGE ADR	LINE ADR	INSTR.	LABEL	INSTR.	MODIFIER		COMMENTS
FF	F0	3E	TO EXP	LDAI		PRI MEM	JUMP TO EXPANDED MEMORY
	1	01		—	01		
	2	D3		OPA			
	3	XX		—			PORT ADDRESS
	4	E9		JPN	HL	EXP. MEM	JUMP TO ADDRESS IN HL
	5						
	6						
	7						
	8	3E	TO PRI	LDAI			JUMP TO PRIMARY MEMORY
	9	00		—	00		
	A	D3		OPA			
	B	XX		—			PORT ADDRESS
	C	E9		JPN	HL	PRI MEM	JUMP TO ADDRESS IN HL
	D						
	E						
	F						
	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
	8						
	9						
	A						
	B						
	C						
	D						
	E						
	F						

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Figure 3-8. 7704 Running Example Four

MEMEX Interrupt Control Software

This last example shows how interrupt service can be handled in a system using MEMEX.

One method previously mentioned is to set aside an area of memory for interrupt service. This area would be permanently enabled.

A second method can be used if the interrupt service routines are short enough. This method has identical service routines in both Primary and Expanded memory. Both routines would reside at the same addresses. This method may, however, use up too much memory space.

A third method is shown in Fig. 3-9, 3-10, and 3-11. In this method, the service routines reside in only one bank of memory. In the example shown, they reside in Primary memory.

The function of the program is to coordinate the jumping to and returning from the interrupt routine. The program ensures that the processor gets to the service routine. If the processor is in Expanded memory, it directs it to switch to Primary memory. It also ensures that the processor returns to the correct bank, after the interrupt is serviced.

The routine resides at address 0024. This is the address an 8085 processor jumps to when it receives a non-maskable interrupt.

Follow the flow chart in Fig. 3-9 and assume that the processor is in Expanded memory when it is interrupted. The processor is directed to select primary memory. It does this by clearing the MEMEX bit in the accumulator and writing it out to the MEMEX port. In Primary memory the processor complements and stores the MEMEX bit. After the interrupt is serviced the MEMEX bit is retrieved. When the bit is output to the MEMEX port, the processor is returned to Expanded memory. It then returns to the program from which it was interrupted.

If the processor is in Primary memory when it is interrupted, it sets the MEMEX bit in the accumulator to a one. It is then complemented and stored. After the interrupt is serviced, the MEMEX bit is retrieved and is output to the MEMEX port. The MEMEX line is already low, however, so this has no effect. The processor simply continues in Primary memory. It then returns to the program from which it was interrupted.

Figures 3-10 and 3-11 show how this program could be written. The program in Fig. 3-10 would reside in Primary memory, and the program in Fig. 3-11 in Expanded memory. This program should reside at each address where an interrupt service routine is located.

HEXADECIMAL			MNEMONIC			TITLE MEMEX + INTER	DATE
PAGE ADR	LINE ADR	INSTR.	LABEL	INSTR.	MODIFIER		COMMENTS
00	20						
	1						
	2						
	3						
	24	3E	(MEMEX + INTER)	LDAI			SET MEMEX BIT IN ACCUMULATOR
	5	01		—	01		
	6	00		NOP			
	7	00		NOP			
	8	2F		CMA			COMPLIMENT AND STORE MEMEX BIT
	9	F5		PSP	AF		
	A	C3		JP	UN	P	SKIP OVER EXIT TO INTER
	B	31		—		R	
	C	00		—	INTER	I	
	D	F1	EXIT	PLP	AF	M	RETRIEVE AND OUTPUT MEMEX BIT
	E	D3		OPA		A	
	F	XX		—		RY	← PORT ADDRESS
00	30	C9		RTS		M	EXIT PRIMARY MEMORY
	1	XX	INTER			EM	INTERRUPT SERVICE
	2	XX				O	
	3	XX				R	
	4	XX				Y	
	5	XX					
	6	XX					
	7	XX					
	8	XX					
	9	XX					
	A	XX					
	B	XX					
	C	XX					
	D	C3		JP	UN		GO EXIT
	E	2D		—			
	F	00		—	EXIT		

Figure 3-9. MEMEX, Interrupt Software, Primary Memory

HEXADECIMAL			MNEMONIC			TITLE MEMEX + INTER	DATE
PAGE ADR	LINE ADR	INSTR.	LABEL	INSTR.	MODIFIER		COMMENTS
00	20						
	1						
	2						
	3						
	24	3E	(MEMEX + INTR)	LDAI			CLEAR AND OUTPUT MEMEX BIT,
	5	00		—	00		SELECTS PRIMARY MEMORY
	6	D3		OPA			
	7	XX		—			← PORT ADDRESS
	8	00		NOP			UNUSED
	9	00		NOP		E	
	A	00		NOP		X	
	B	00		NOP		P	
	C	00		NOP		A	
	D	00		NOP		N	
	E	00		NOP		D	
	F	00		NOP		ED	
	30	C9		RTS			EXIT (EXPANDED MEMORY)
	1					M	
	2					E	
	3					M	
	4					O	
	5					R	
	6					Y	
	7						
	8						
	9						
	A						
	B						
	C						
	D						
	E						
	F						

Figure 3-10. 7704, MEMEX, Interrupt Software Expanded Memory

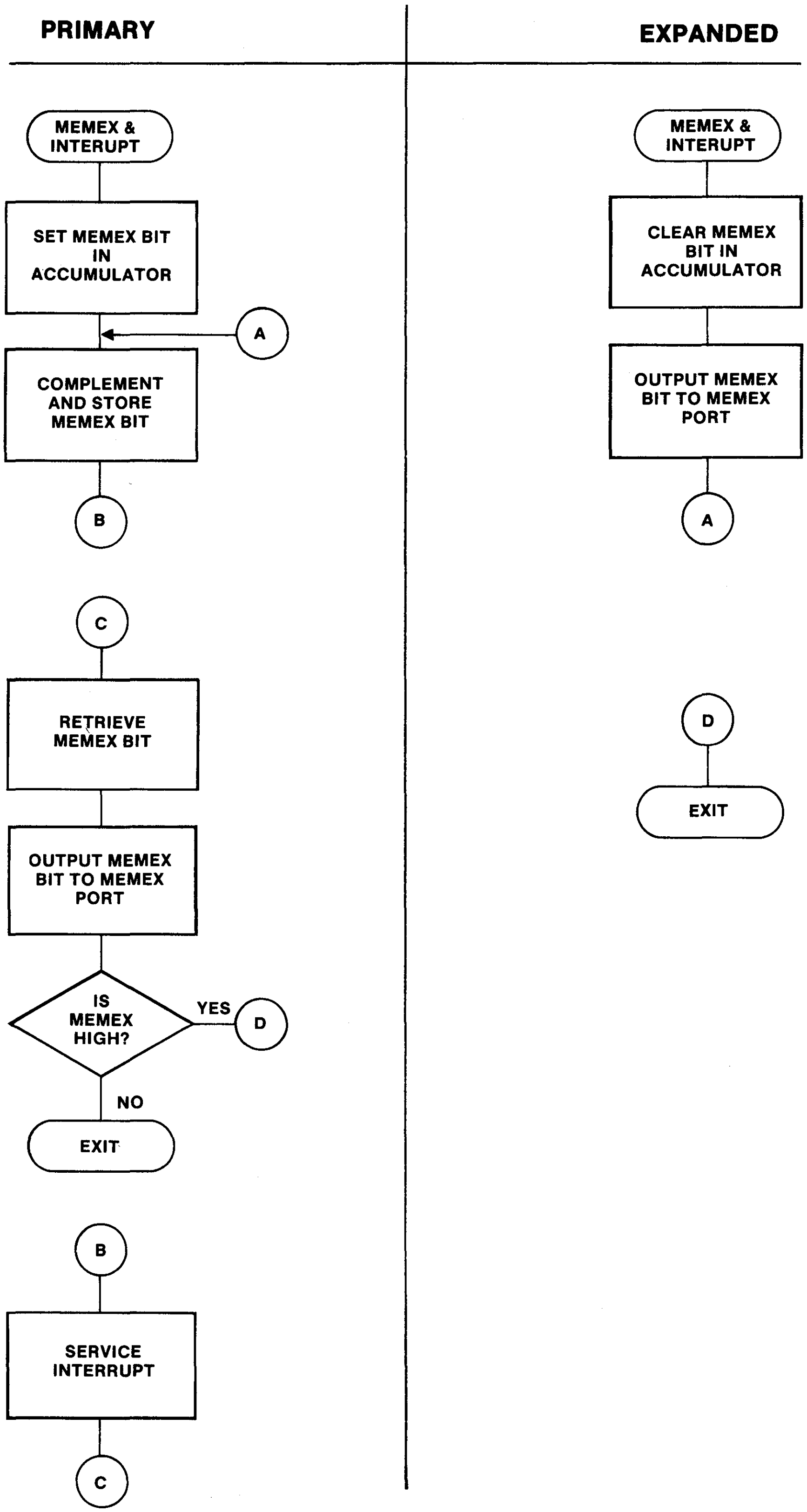


Figure 3-11. 7704, MEMEX, Interrupt Software Flowchart

Segment Select

The Segment Select line is not a part of the STD BUS but is an external line which must be connected on the card ejector side of the 7704 when used. Fig. 2-2 shows the location of the connector. The purpose of the line is to allow the 7704 card to participate in large scale memory bank select schemes where multiple cards occupy the same address field.

Whereas the MEMEX line can be used to select one of two banks of memory, the Segment Select line can choose one of any number of memory banks.

The line is normally controlled by a memory segment controller or by output ports. An I/O card such as Pro-Log's 7605 card along with an RC704 cable can be used to control the line. One output port can control eight cards.

Figure 3-12 is an example of how the line can be used. It shows a 184K memory system with 4K RAM and 180K ROM. The 4K RAM is on the processor card and is permanently enabled. The 180K ROM is on three cards. Each card has its Segment Select line connected to a bit of an output port on an I/O card. All three cards occupy the same address field.

At power up the output port bits would be low. One of the 7704 cards would be configured for low level active Segment Select. The other two would be high level active. Therefore, one of the cards would automatically be selected at power up. The processor could thereafter choose which card it wanted simply by writing to the output port.

A second example shows how MEMEX and Segment Select can be combined. Normally, MEMEX will be used if possible, since it requires no additional lines. If Segment Select is used, MEMEX would probably not be used. However, they can be used together.

In Fig. 3-13, and 84K system is shown. It has 12K of ROM and 2K of RAM on the processor card. This memory is permanently enabled, and could hold the main program, including software for controlling MEMEX and Segment Select.

The rest of the memory is in four banks on two 7704 cards. Each bank uses approximately the same address space. Note that each bank has a different combination of ROM and RAM. Each bank could be dedicated to a specific job that the processor has to do. For instance, in an interrupt system, the processor could use a different bank to service each interrupt. The memory combination of each bank could be tailored to suit the specific job that it will be used for.

The processor card is a Pro-Log 7804 card. It has one output line which is used here for Segment Select. This one Segment Select line is connected to both 7704 cards. The one marked Segment One is enabled when Segment Select is low. The one marked Segment Two is enabled when Segment Select is high.

On the card marked Segment One, one bank is enabled when MEMEX is low, and one when it is high. The same is true for the card marked Segment Two. The processor selects one segment, or card by setting the Segment Select line high or low. It then selects which of the banks on the card is enabled by setting the MEMEX line high or low.

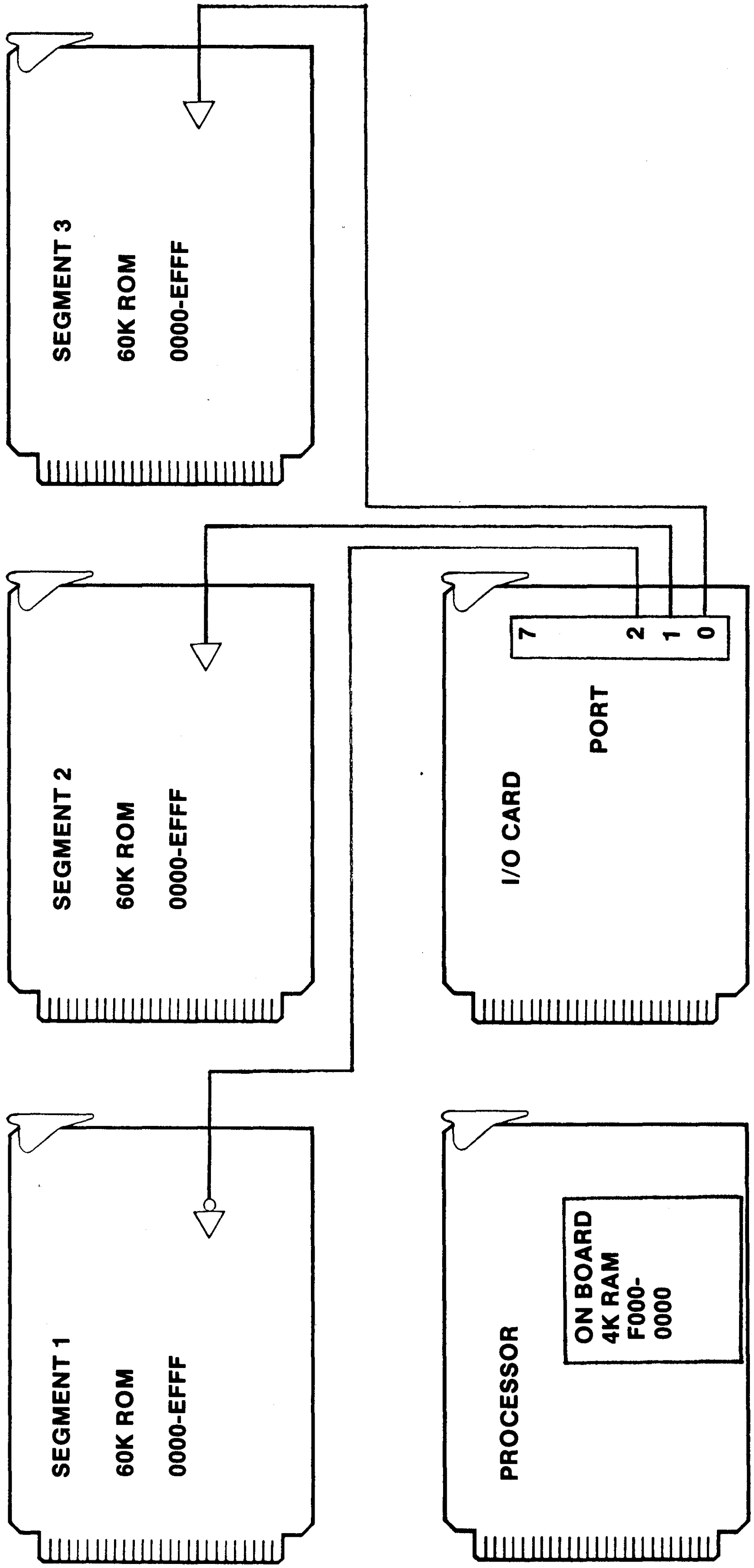


Figure 3-12. 7704 Segment Select Example One

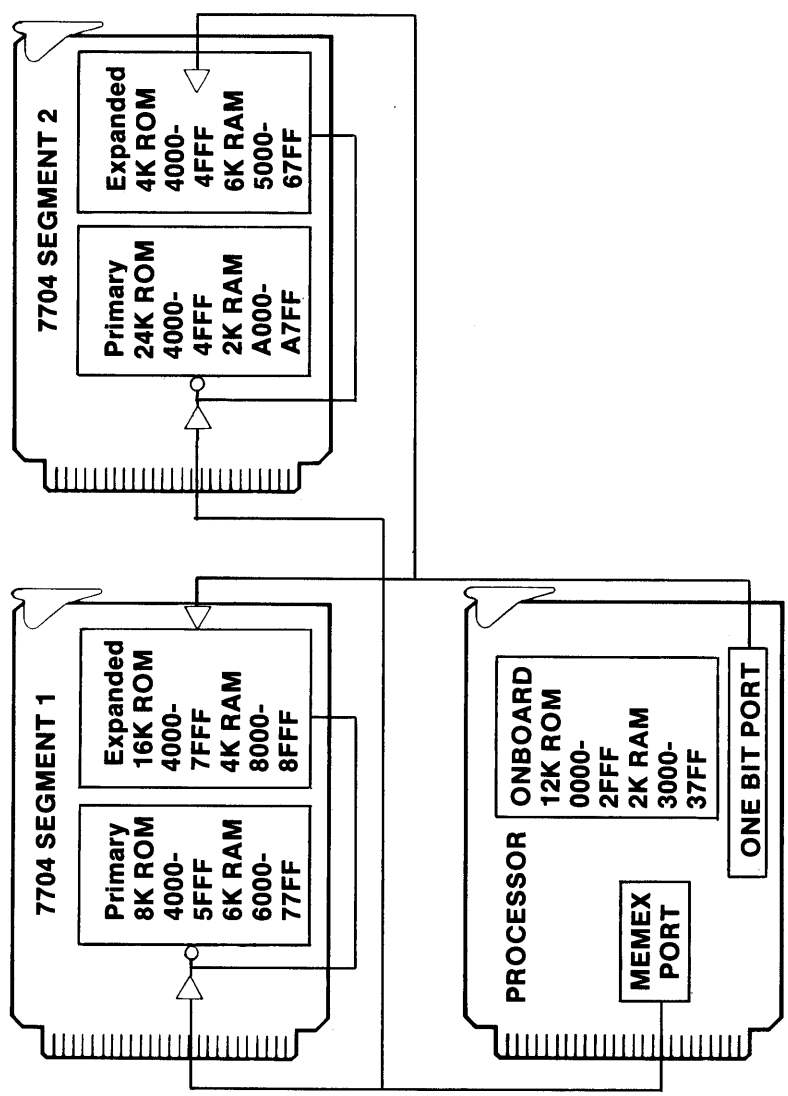


Figure 3-13. 7704 Segment Example Two

Segment Select Control Software

The control software for Segment Select is very similar to that used for MEMEX. The difference is, that it must be able to control more than two Segments. To do this, the program must be told what Segment to jump to. It must also be told what Segment to return to.

As with MEMEX, many applications will require an area of Permanent memory. The simplest Segment Control software would reside in this area. Figure 3-14 is an example of such a program.

It is similar to the program in MEMEX Software Example One. It coordinates jumping from one Segment to a subroutine in another Segment. The difference here is that you must enter the program with two additional variables. Register A must have the number of the Segment you are jumping to. Register B must have the number of the Segment you are jumping from.

The "number" of the segment would be either 01, 02, 04, 08, 10, 20, 40, or 80 HEX. One bit for each segment. This program can therefore control up to eight segments.

Any of the MEMEX control software examples can be adapted for Segment Control. Or entirely different control software can be written. Use these as examples from which to write your own programs.

HEXADECIMAL			MNEMONIC			TITLE SEGMENT CONTROL DATE	
PAGE ADR	LINE ADR	INSTR.	LABEL	INSTR.	MODIFIER		COMMENTS
FF	F 0	D3		OPA			SWITCH TO DESIRED SEGMENT
	1	XX		—			← PORT ADDRESS
	2	C5		PSP	BC		SAVE ORIGINAL SEGMENT NUMBER
	3	E5		PSP	HL		PUSH RETURN ADDRESS ONTO TOP OF
	4	21		LDPI	HL		STACK (FFF9)
	5	F9		—			
	6	FF		—			
	7	E3		XCPT	HL		
	8	E9		JPN	HL		JUMP TO SUBROUTINE AT H.L
FF	F 9	C1		PLP	BC	PERMANENT	RETURN TO ORIGINAL SEGMENT
	A	78		LDA	B		
	B	D3		OPA			
	C	XX		—			← PORT ADDRESS
	D	C9		RTS			EXIT
	E						
	F						
	0						
	1					MEMORY	
	2						
	3						
	4						
	5						
	6						
	7						
	8						
	9						
	A						
	B						
	C						
	D						
	E						
	F						

Figure 3-14. 7704 Segment Control Software

SECTION 4

Operating Software

Section 4 is usually reserved for software for operation of an STD Series 7000 card. The 7704 card requires no software except for those examples given in Section 3.

Reference Drawings

The schematic (Fig. 5-1) and assembly drawing (Fig. 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. They may differ in some respects from the card and documentation that the user receives from Pro-Log.
The schematic and the assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.

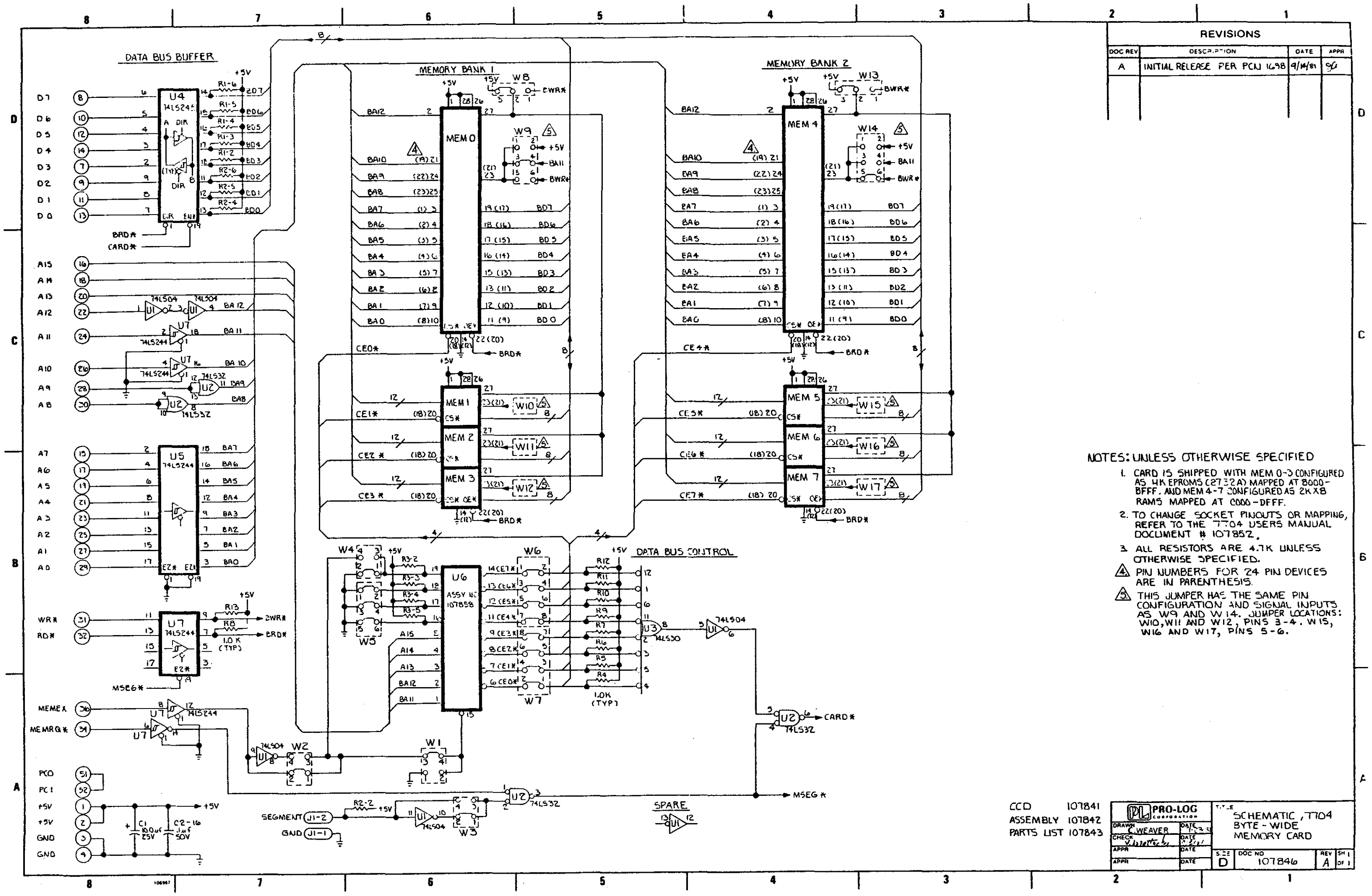


Figure 5-1. 7704 Schematic

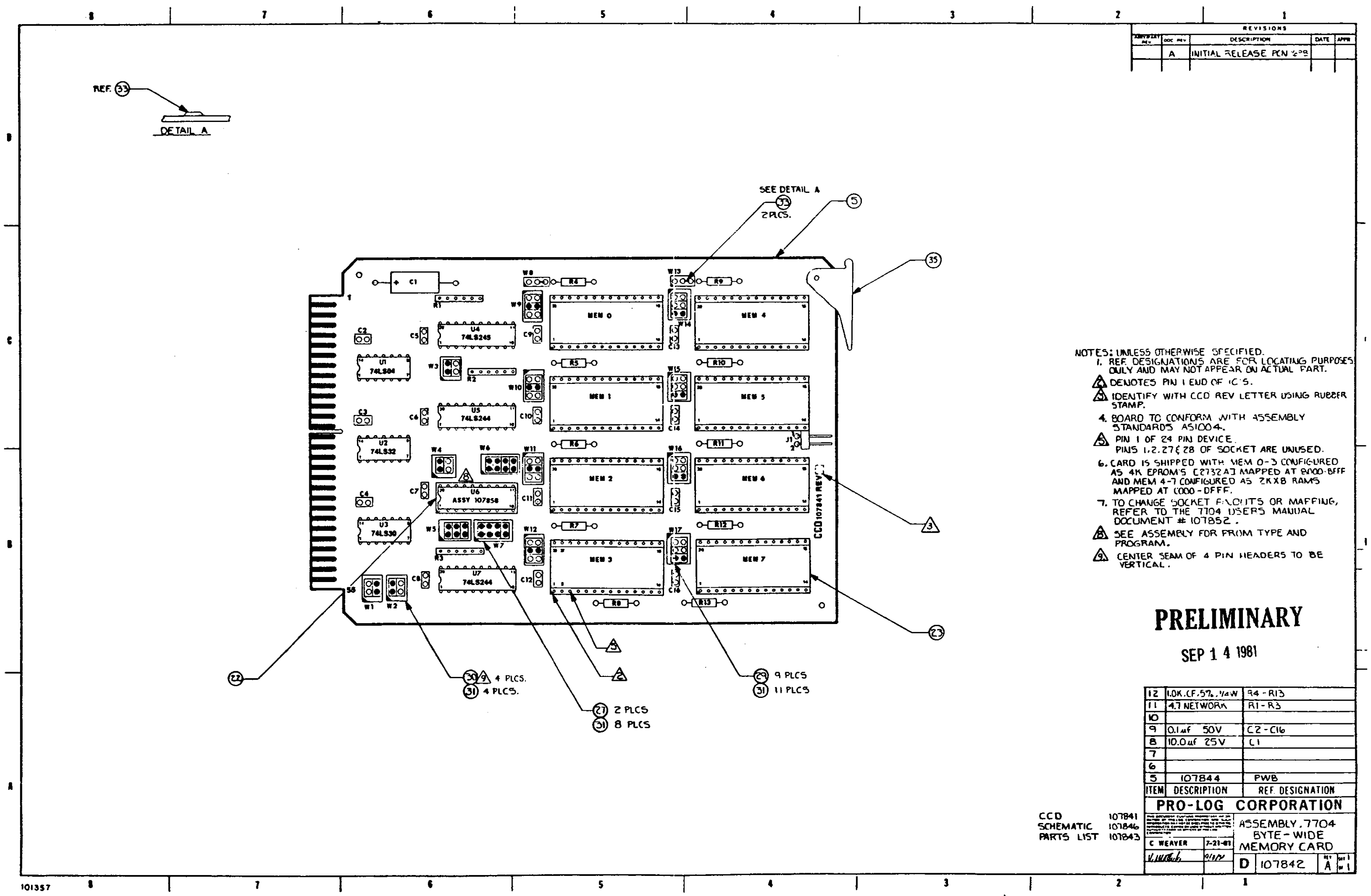


Figure 5-2. 7704 Assembly

Return for Repair Procedures

Domestic Customers:

1. Call our factory direct at (408) 372-4593, and ask for CUSTOMER SERVICE.

2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, reason for return, and the name and telephone number of the person we should contact (preferably the user), if we have any further questions.

4. Package the equipment in a solid cardboard box secured with packing material.

   CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, CA 93940

   Reference CRO # __________.

International Customers:

Equipment repair is handled by your local Pro-Log Distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty: Seller warrants that the articles furnished hereunder are free fom defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part, whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced bo Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

USER'S MANUAL

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